MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC – AUTONOMOUS INSTITUTION)

Estd: 1998

(Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi)
www.mits.ac.in

Schedule -M. Tech (VLSI Design & Embedded Systems) II Year I Semester (R24) Mid- Term Test -II December -2025

Academic Year – 2025-2026 (For 2024 Admitted batch)

Skill Enhancement Course

Branch	Date &Day	Session &Time	Roll Nos	Course Name /Code	Lab No
M.Tech	18.12.2025 (Thursday)	AN: 02:00 PM-04:00 PM	24691D6901-24691D6915	QNX Embedded Real Time Operating System (24VESP601)	LB-202

CONTROLLER OF EXAMINATIONS

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MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE
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PRINCIPAL

Principal
Madanapalle Institute of
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MADANAPALLE